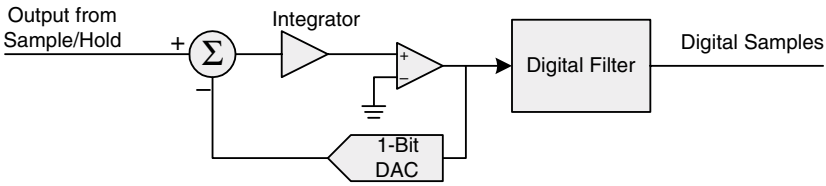

FIGURE 15.12 Sigma-delta ADC circuit.

less than 0, the comparator's output is 0, and there is no negative feedback, causing the running difference to increase once again.

The disadvantage of a sigma-delta ADC is that it requires a high oversampling frequency to function. However, this is not a problem at low frequencies, such as audio, where these converters are commonly employed. A sigma-delta ADC is able to deliver very high resolutions (e.g., 24 bits) with high accuracy, because most of its complexity is in the digital filter, and only a coarse single-bit conversion is performed. This means that the circuit is less susceptible to noise. Digital logic is much more tolerant of ambient noise as compared to delicate analog comparators and amplifiers.

A key advantage of sigma-delta ADCs for the system designer is that expensive lowpass filters with sharp roll-offs are not required. Since the actual sampling frequency is so much higher than the signal's frequency content, an inexpensive single-pole RC lowpass filter is generally sufficient. Consider a CD audio sampling application in which the maximum input frequency is 20 kHz and the nominal sampling rate is 44.1 kHz. A sigma-delta ADC might sample this signal at 128×44.1 kHz = 5.6448 MHz. Therefore, the Nyquist frequency is raised to approximately 2.8 MHz from 22 kHz! A first-order filter with f_C = 20 kHz would attenuate potentially aliasing frequencies by more than 40 dB. In contrast, a normal ADC would require a much more costly filter to provide the same attenuation where the passband and stopband are separated by only 2 kHz.

15.4 DAC CIRCUITS

Unlike an ADC, a DAC does not require a sample and hold circuit, because the instantaneous sample events are driven from the discrete digital domain where each clock cycle activates a new sample. A DAC consists of a digital interface and the conversion circuit. Two of the most common types of conversion circuits are the *R-2R ladder* and sigma-delta designs.

The R-2R ladder DAC uses the concept of current summation as found in an inverting op-amp summing circuit. Two resistance values, R and 2R, are connected in a multistage network as shown in Fig. 15.13 (using a four-bit example for the sake of brevity). This circuit is best analyzed using superposition: set one input bit to logic 1 (V_{REF}) and the others to logic 0 (ground). When this is done, the resistor ladder can be quickly simplified by combining parallel and series resistances, because all nodes other than the logic 1 input are at 0 V. Knowing that the voltage at the op-amp's negative terminal is also 0, the current through the resistor ladder can be determined and, therefore, the output voltage can be calculated.

After calculating the partial output voltage due to each individual input, the following overall expression for V_O is obtained:

$$V_O = -V_{REF}\left[\frac{D3}{2} + \frac{D2}{4} + \frac{D1}{8} + \frac{D0}{16}\right]$$

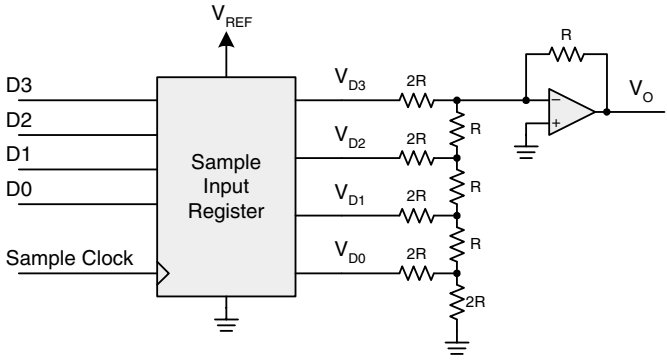

FIGURE 15.13 Four-bit R-2R ladder DAC.

This expression allows linear control of V_O ranging from 0 to within one least-significant bit position (1/16 in this case) of $-V_{REF}$. Similar results can be obtained with the basic op-amp summer circuit, but each input bit's resistor must be twice the value of the previous bit's resistor. This rapidly becomes impractical with 8, 12, 16, or more bits of resolution.

Real DACs modify this basic circuit to generate positive output voltage ranges. In actuality, the basic R-2R ladder concept is often used, but the exact circuit topology and current summation mechanism change to better suit circuit design constraints. Many R-2R ladder DACs are designed to emit the summed currents rather than a voltage and therefore require an external op-amp circuit to create the final desired signal. This requirement is not really burdensome, because a buffer of some type is usually needed to provided sufficient drive strength to the intended load. A DAC is designed to reconstruct analog signals with accuracy, but not to drive substantial loads. Therefore, even a voltage-output DAC may require a unity gain op-amp stage for the system to function properly. A current-output DAC can be connected in a manner similar to that shown in Fig. 15.14. Assuming that the output range is 0 to 10 mA, this circuit is capable of V_O from 0 to 4.99 V. The DAC is designed to sink rather than source current so that the inverting op-amp configuration produces a positive output voltage.

A sigma-delta DAC operating principle is similar to that of the sigma-delta ADC. An internal digital filter converts multibit samples (e.g., 16 bits) at the desired rate into single-bit samples at a high-frequency multiple of that rate. Over time, the average DC value of these high-frequency samples corresponds to the desired DAC output voltage. This high-frequency signal is filtered to yield a converted analog signal with minimal distortion. As with an ADC, a sigma-delta DAC has the advantage of requiring an inexpensive lowpass filter, because the sampling rate is so much higher than the fre-

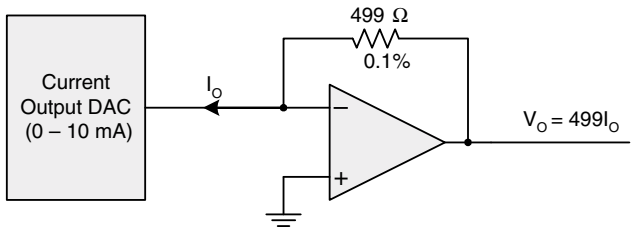

FIGURE 15.14 Buffered current-output DAC.